UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,717	10/23/2003	Kiyokuni Kawachiya	JP920020196US1	6813

48243 7590 01/04/2007

FLEIT, KAIN, GIBBONS, GUTMAN, BONGINI & BIANCO PL
551 NW 77TH STREET,
SUITE 111
BOCA RATON, FL 33487

EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/691,717	KAWACHIYA ET AL.	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15,17,19 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-13,15,17,19 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 12/02/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zolnowsky (US5826081) in view of Wah Chan et al (US20020046334) hereinafter Wah Chan.

3. As to claim 1, Zolnowsky discloses an exclusion controller which allows an information processing unit to acquire a contended resource to the exclusion of other information processing units, the exclusion controller comprising: a plurality of non-prioritized information processing units mutually exclusively acquiring a non-prioritized exclusion right by a first process, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource (Figure 5 illustrates said controller controlling high priority queue 501 that allows the selected thread to access shared resource 503, excluding other threads. These steps are shown in figure 7, steps 701 and 702, Col. 8, lines 14 – 18); and

Zolnowsky does not explicitly disclose the first process executing writes using compare and swap instruction.

However, Wah Chan teaches of using the swap and compare instruction prior to the locking of the resource by any particular CPU as illustrated in Figure 1, page 1, paragraph 0019.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the atomic instruction mode of Wah Chan in the multiprocessor system of Zolnowsky to improve the data flow efficiency of said system, page 1, paragraph 0003). One of ordinary skill in the art would have been motivated to use the atomic instruction mode of Wah Chan in the multiprocessor system of Zolnowsky to improve the data flow efficiency of said system, page 1, paragraph 0003).

Wah Chan also teaches of a prioritized information processing unit acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the second process executing writes by using normal write instructions.
When the CPU selected has locked the resource, the normal write sequence is used , page 2, paragraph 0034.

4. As to claim 2, Zolnowsky discloses the exclusion controller, further comprising: a prioritized exclusion right storage area for storing prioritized exclusion right information indicating that the prioritized information processing unit is trying to acquire the contended resource (Figure 4A illustrates a storage area, queue 404, associated with controller processor N (403) that stores required thread, COL. 6, lines 30 – 35); and

a non-prioritized exclusion right storage area for storing non-prioritized exclusion right information indicating which of the plurality of non-prioritized information processing units has acquired the non-prioritized exclusion right, wherein each non-prioritized information processing unit executes, as the first process, a process for storing the non-prioritized exclusion right information indicating that the non-prioritized information processing unit has acquired the non-prioritized exclusion right, to the exclusion of the other non-prioritized information processing units if the non-prioritized exclusion right information has not yet stored, and the prioritized information processing unit executes, as the second process, a process for storing the prioritized exclusion right information and then reading the non-prioritized exclusion right storage area, and acquires the contended resource if the non-prioritized exclusion right information is not stored, but does not acquire the contended resource if the non-prioritized exclusion right information has already stored (Figure 4A illustrates processor 1, processor 2, as non-prioritized processing unit comprising queues such as 401 that comprises the non-prioritized threads, COL.6 , lines 30 – 52).

5. As to claim 3, Zolnowsky discloses the exclusion controller, further comprising: an area usage type storage area for storing information indicating which of the non-prioritized exclusion right information or prioritized information processing unit information the non-prioritized exclusion right storage area stores, wherein the non-prioritized exclusion right storage area stores any one of the non-prioritized exclusion

right information and the prioritized information processing unit information indicating which of the plurality of information processing units is the prioritized information processing unit, and each of the prioritized information processing unit and the plurality of non-prioritized information processing units acquires the non-prioritized exclusion right by the first process if the non-prioritized exclusion right storage area stores the non-prioritized exclusion right information, and the information processing unit acquires the contended resource if the information processing unit has acquired the non-prioritized exclusion right (Figure 5 illustrates the acquisition of the shared resource, memory 503 by having the scheduler 1 through scheduler N afford said capture based on the requisite of the high priority real time queue 501, Col. 7, lines 25 – 34).

6. As to claim 4, Zolnowsky discloses the exclusion controller, further comprising a prioritized information processing unit change unit for changing the prioritized information processing unit into a non-prioritized information processing unit if non-prioritized exclusion right information has been already stored, in the second process (Figure 5 illustrates a series of schedulers enabled by the high priority policy of real time queue 501 that can shift from processor 1 to processor n dependent on the policy being executed, , COL. 7, lines 25 – 34).

7. As to claim 5, Zolnowsky discloses the exclusion controller, further comprising: an acquisition check unit for checking whether the acquisition of the contended resource

by any one of the first and second processes has failed (Figure 6 illustrates the checking for acquisition of the resource in step 604, COL. 7, line 65 – Col. 8, line 12) ; and a monitor control unit for executing exclusion control by a monitor mode in which all the information processing units waiting to acquire the contended resource are previously recorded and the information processing unit having released the contended resource notifies the information processing units waiting to acquire the contended resource that the contended resource has been released, if a check has been made that the acquisition of the contended resource has failed (Figure 6, step 601 illustrates the selection of a thread from all contenting processors, thus a notification scheme need to be in place to allow such notification, COL. 7, lines 55 – 64).

8. As to claim 6, Zolnowsky discloses the exclusion controller, further comprising: a prioritized information processing unit information storage area for storing prioritized information processing unit information indicating which of the information processing units is the prioritized information processing unit; and a prioritized information processing unit setting unit for allowing any one of the plurality of information processing units to execute a process for storing, in the prioritized information processing unit information storage area, the prioritized information processing unit information indicating that the information processing unit is the prioritized information processing unit, to the exclusion of the other information processing units if the prioritized

information processing unit information has not been stored (Figure 5 illustrates the high priority queue 501 that comprises said storage function, COL. 7, lines 20 – 23).

9. As to claim 7, Zolnowsky discloses the exclusion controller, further comprising a prioritized information processing unit setting unit for setting the information processing unit having first acquired the contended resource as the prioritized information processing unit and for setting the other information processing units except the prioritized information processing unit as the non-prioritized information processing units (The scheduling variable that pre-empts the other processors can be executed to deliver said configuration, COL. 7, lines 15 – 30).

10. As to claim 8, Zolnowsky discloses the exclusion controller, further comprising a prioritized information processing unit change unit for changing any one of the non-prioritized information processing units into the prioritized information processing unit (Scheduling variable can enable said configuration, COL. 7, lines 24 – 34).

11. As to claim 9, Zolnowsky discloses the exclusion controller, further comprising: a full stop unit for stopping all of the plurality of information processing units, wherein the prioritized information processing unit change unit changes the non-prioritized information processing unit having acquired the contended resource at the time when all of the plurality of information processing units are stopped, into the prioritized

information processing unit (Scheduling variable in each processor afford said configuration, COL. 7, lines 24 –34).

12. As to claim 10, Zolnowsky discloses the exclusion controller, further comprising:
a resource information storage area for storing resource information indicating whether the contended resource has been acquired by any one of the plurality of information processing units, while associating the resource information with
priority right information indicating that the prioritized information
processing unit exists, wherein the prioritized information processing unit
executes, as the second process, a process for reading information from the
resource information storage area and for writing the resource information in
the resource information storage area if the priority right information is
stored, and wherein each non-prioritized information processing unit comprises:
a prioritized information processing unit stop unit for stopping the
prioritized information processing unit (Processor controlling high priority queue which comprise the variable to stop prioritized processor, COL. 7, lines 24 –34);
a priority right removal unit for removing the priority right information from the resource information storage area by the first process exclusively from the other information processing units after the prioritized information processing unit stop unit has stopped the prioritized information processing unit (Execution of requisite variable would afford said action, COL. 7, lines 24 –34);

a transient state check unit for checking whether the stopped prioritized information processing unit is executing the second process (Figure 6, step 602); and

an execution state setting unit for setting an execution state of the prioritized information processing unit to a state in which the prioritized information processing unit is not acquiring the contended resource by the second process, if a check has been made that the prioritized information processing unit is executing the second process (figure 6, step 604).

13. As to claim 11, Zolnowsky discloses the exclusion controller, wherein the execution state setting unit sets the execution state by setting execution location information indicating an execution location of a program realizing the prioritized information processing unit to be in a state before the resource information storage area is read (Setting processor variables can achieve said configuration, COL. 7, lines 24 – 34).

14. As to claim 12, Zolnowsky discloses the exclusion controller, wherein the execution state setting unit invalidates a process for writing in the resource information storage area in the second process (Setting processor variables can achieve said configuration, COL. 7, lines 24 – 34).

15. As to claim 13, Zolnowsky discloses the exclusion controller, further comprising a monitor control unit for executing exclusion control by a monitor mode in which all the information processing units waiting to acquire the contended resource are previously recorded and the information processing unit having released the contended resource notifies the information processing units waiting to acquire the contended resource that the contended resource has been released, if information indicating that the prioritized information processing unit does not exist has been stored in the resource information storage area (Figure 5 illustrates a queue 501, comprising said information, COL. 7, lines 15 – 23).

16. As to claims 15 and 19, Zolnowsky discloses an exclusion control method and recording medium for allowing an information processing unit to acquire a contended resource to the exclusion of other information processing units, the exclusion control method comprising: a plurality of non-prioritized information processing modules for mutually exclusively acquiring a non-prioritized exclusion right by a first process, the non-prioritized exclusion right indicating a candidate for acquiring the contended resource (Figure 3 shows the recording medium such as mass storage unit 315 and figure 5 illustrates the plurality of non-prioritized processing modules 507,513, 519 contending for exclusive access to shared memory 503. Said contention is enabled by the associated dispatcher, such as 509., COL. 7, lines 15 - 20;

Zolnowsky does not explicitly disclose the first process executing writes using compare and swap instruction.

However, Wah Chan teaches of using the swap and compare instruction prior to the locking of the resource by any particular CPU as illustrated in Figure 1, page 1, paragraph 0019.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the atomic instruction mode of Wah Chan in the multiprocessor system of Zolnowsky to improve the data flow efficiency of said system, page 1, paragraph 0003). One of ordinary skill in the art would have been motivated to use the atomic instruction mode of Wah Chan in the multiprocessor system of Zolnowsky to improve the data flow efficiency of said system, page 1, paragraph 0003).

Wah Chan also teaches of a prioritized information processing unit acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the second process executing writes by using normal write instructions.
When the CPU selected has locked the resource, the normal write sequence is used , page 2, paragraph 0034.

17. As to claim 17, Zolnowsky discloses a program for causing a computer to function as an exclusion controller, which allows an information processing unit to acquire a contended resource to the exclusion of other information processing units, the program causing the computer to effect the functions (Zolnowsky teaches of application loaded into the operating system kernel to execute program, COL. 5, lines 26 – 38).

18. As to claim 18, Zolnowsky discloses a program for causing a computer to function as an exclusion controller which allows any one of a plurality of threads capable of acquiring an identical contended resource to acquire the contended resource to the exclusion of the other threads different from the relevant thread, the program causing the computer to effect the functions (Zolnowsky teaches of application loaded into the operating system kernel to execute program, COL. 5, lines 26 – 38).

19. As to claim 21, Zolnowsky discloses a computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing exclusion control, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect the functions (Zolnowsky teaches of application loaded into the operating system kernel to execute program, COL. 5, lines 26 – 38).

20. As to claim 22, Zolnowsky discloses a computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing exclusion control, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect the functions (Zolnowsky teaches of application loaded into the operating system kernel to execute program, COL. 5, lines 26 – 38).

21. As to claim 23, Zolnowsky discloses an article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing exclusion control, the computer readable program code means in said article of manufacture comprising computer readable program code means for causing a computer to effect the steps (Figure 3 illustrates mass storage unit 315 which comprises program code to effect computer operation, COL. 5, lines 26 – 38).

22. As to claim 24, Zolnowsky discloses a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for exclusion control, said method steps comprising the steps (Figure 3 illustrates mass storage unit 315 which comprises program code to effect computer operation, COL. 5, lines 26 – 38).

Response to Arguments

23. Applicant's arguments with respect to claims 1,15, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Zolnowsky does not explicitly disclose the first process executing writes using compare and swap instruction.

Wah Chan teaches of using the swap and compare instruction prior to the locking of the resource by any particular CPU as illustrated in Figure 1, page 1, paragraph 0019.

Wah Chan also teaches of a prioritized information processing unit acquiring the contended resource by a second process to the exclusion of the non-prioritized

information processing unit having acquired the non-prioritized exclusion right, the second process executing writes by using normal write instructions.

When the CPU selected has locked the resource, the normal write sequence is used , page 2, paragraph 0034.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAD
12/20/2006

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100